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Mazumder, P.;
Test Conference, 1988. Proceedings. 'New Frontiers in Testing'., International
12-14 Sept. 1988 Page(s):279 - 288
Digital Object Identifier 10.1109/TEST.1988.207812

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☐ 2. **Design of a fault-tolerant three-dimensional dynamic random-access mer chip error-correcting circuit**
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☐ 3. **Pattern sensitive fault testing of RAMs with built-in ECC**
Franklin, M.; Saluja, K.K.;
Fault-Tolerant Computing, 1991. FTCS-21. Digest of Papers., Twenty-First Inte
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Gregori, S.; Khouri, O.; Micheloni, R.; Torelli, G.;
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Digital Object Identifier 10.1109/MTDT.2001.945227

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☐ 5. **120-ns 128 K*8-bit/64 K*16-bit CMOS EEPROMs**
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7. **Do we need anything more than single bit error correction (ECC)?**
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9. **A sub-0.5-V operating embedded SRAM featuring a multi-bit-error-immun
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11. **Adding error-correcting circuitry to ASIC memory**
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☐ 13. **A 5 V only one-transistor 256 K EEPROM with page-mode erase**
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